

31002 U.S. PTO
10/055568
01/22/02

PATENT NUMBER and
ISSUE DATE

U.S. UTILITY Patent Application

APPL NUM 10055568	FILING DATE 01/22/2002	CLASS 257	SUBCLASS 411	GAU 2841	EXAMINER 11
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****APPLICANTS:** Lin Mou-Shiung; Lee Jin-Yuan; Huang Ching-Cheng;

****CONTINUING DATA VERIFIED:**

**** FOREIGN APPLICATIONS VERIFIED:**
TAIWAN 90123195 12/31/2001

PG-FUB	DO NOT PUBLISH <input type="checkbox"/>	RESCIND <input type="checkbox"/>
Foreign priority claimed <input type="checkbox"/> Yes <input type="checkbox"/> No 35 USC 119 conditions met <input type="checkbox"/> Yes <input type="checkbox"/> No Verified and Acknowledged Examiners' initials		ATTORNEY DOCKET NO JUL 2533
TITLE : Integrated chip package structure using silicon substrate and method of manufacturing the same		

NOTICE OF ALLOWANCE MAILED		Assistant Examiner	CLAIMS ALLOWED	
			Total Claims	Print Claim for O.G.
ISSUE FEE		Primary Examiner	DRAWING	
Amount Due	Date Paid		Sheets Drwg.	Figs. Drwg.
<input type="checkbox"/> TERMINAL DISCLAIMER		PREPARED FOR ISSUE	Application Examiner	
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